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METHODS OF DETERMINING INTEGRAL ADC DYNAMIC CHARACTERISTICS

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Keywords: differential non-linearity; dynamic characteristics; effective number of bits; instantaneous dynamic errors; integral ADC; integral non-linearity.

Abstract: The article offers methods to determine instantaneous dynamic errors of integral analog-to-digital converters and effective number of bits. The first method is to compare registered signal of known form at the output of the ADC tested with the model of this form, formed by computer. Effective number of bits is defined from experimental data by the error that occurs in each point of ADC dynamic range depending on the specified rate of test signal change or on its frequency.

Introduction

Widespread application of various devices for analog-to-digital conversion (**ADC**) of electrical signals in digital oscillography, radio engineering devices, medical diagnostic equipment, etc. causes the developers of such equipment to learn such actual metrological characteristics of applied integral ADCs, especially dynamic ones as:

– Total Harmonic Distortion (**THD**);
– Signal to Noise Ratio (**SNR**);
– Signal to Noise and Distortion (**SINAD**);
– Effective Number of Bits (**ENOB**);
– Spurious Free Dynamic Range (**SFDR**).

The relevance of evaluating dynamic ADC characteristics is also caused by the fact that the market of integral ADC is full of various devices that have common characteristics but different producers.

A Wide variety of ADC devices manufactured mainly abroad by different countries and companies is used in Russia [1]. Manufacturers make use of their own methods and standards when determining ADC metrological characteristics [2, 3] that should be brought into line with our Russian standards for these devices to enter the register of measuring instruments of the Russian Federation with the aim of their further usage. The problem is complicated by the fact that the dynamic characteristics mentioned above are not given in the State Standards of Russian Federation [4] and the existing methods to determine dynamic errors [5] provide only averaged statistical estimates which are known to level out some significant outliers of instantaneous errors causing low confidence of customers for such estimates. Therefore, all abovementioned facts lead to the task of determining ADC instantaneous dynamic errors in the entire range of tests in terms of speed and frequency characteristics.

Method of determining ADC instantaneous dynamic errors

The main idea of this method is to compare registered signal of known form $x[j]$ at the output of the ADC tested with the model of this form $M[j]$, formed by computer.

A calibrated signal generator (**CSG**) is used as a test signal source. To do this we can use verification – purpose generator of harmonic oscillations with minimum non-linear distortions. The signal from the generator is fed to the ADC tested. ADC codes are transmitted to buffer storage device in the form of the array with sufficient size. The whole array has to fit within at least one period of test harmonic signal.

As signal $x[j]$ has harmonic form, then this model needs to have four parameters: amplitude A, offset S, period T and initial phase φ. These parameters may be read from CSG and entered to computer (without phase) but the error of setting test signal informative parameters into CSG and ADC statistical errors (such as offset, conversion factor, etc.) will lead to significant distortions of measurement results.

Therefore, another method of determining these parameters based on their measurement directly from a registered signal has been adopted. To do this we need to determine time number t_i of extrema $x(t_i)$ for the signal registered and the number of extrema being the basis to determine:

Amplitude: $A = \frac{1}{2(n-1)} \sum_{i=1}^{n-1} \left[x(t_i) - x(t_{i+1}) \right]$;

Offset: $S = \frac{1}{2(n-1)} \sum_{i=1}^{n-1} \left[x(t_i) + x(t_{i+1}) \right]$;

Period: $T = \frac{2}{n-1} \sum_{i=1}^{n-1} (t_{i+1} - t_i)$;

Phase: $\varphi = \frac{T}{360} \arcsin\left[2 \frac{x(0) - S}{x(t_i) - x(t_2)} \right]$.

The values received are used as the first approximation to form computer model of a test signal

$$M[j] = A \sin\left[\frac{2\pi}{T} j + \varphi \right] + S.$$

Further approximation is implemented by the least squares method (**LSM**) by iterative procedures with independent increments of A, S, T parameters for φ model by searching minimum value

$$\sum_{i=1}^{n} \left(x[j] - M[j] \right)^2 \to \min .$$

The received model $M[j]$ is accepted as a quasi-original model of a test signal to evaluate dynamic error.

The algebraic difference $\Delta[j] = x[j] - M[j]$ characterizes instantaneous error values of test signal form registration. If test signal non-linearity is really small then the difference $\Delta[j]$ has the following error components:

– ADC differential non-linearity (**DNL**);

– ADC integral non-linearity (**INL**);
– ADC intrinsic noise;
– ADC dynamic errors.

The first three components characterize ADC static accuracy and can be found on the stage of static characteristics tests using abovementioned methods [6, 7].

If static characteristics are found and ADC static conversion function is formed then algebraic difference can be recalculated taking into consideration ADC static errors; the dynamic component only that characterizes instantaneous values of dynamic errors can also be singled out

$$\Delta_d[j] = \Delta[j] - \Delta_s[j].$$

Method of determining ADC ENOB

Effective Number of Bits is considered to be the most important ADC characteristics. It allows showing the total influence of various error sources such as quantization, DNL and INL, non-linear distortions in pre-conversion circuits, sampling dating errors, random instrumental errors, bits losses during dynamic influence. Effective Number of Bits is usually represented as frequency dependent function. In general (but not always) it decreases with frequency increase.

Effective Number of Bits is advisable to be found from experimental data by the error that occurs in each point of ADC dynamic range depending on the specified rate of test signal change or on its frequency. In this case ADC must be put into a mode when dynamic conversion errors are predominant when compared to static ones. Consequently, we need to use a test signal with high slew rate which is typical for ADC when single fast processes are registered. With this approach full dynamic characteristics of input analogue part are not determined allowing to reduce the requirements for test signal since the error in setting its amplitude may not be normalized and the requirements for slew rate accuracy can be significantly reduced. Simultaneously we get the possibility to determine the components of sampling dating errors.

In order to determine experimentally ADC errors in dynamic change mode we need to know exactly instantaneous values of test signal. This can be achieved by means of high-speed reference comparators in combination with slow reference digital-analog converter (**DAC**). When using a single comparator we need to consider its delay. This disadvantage can eliminated with the help of two gated comparators.

The structure of hardware-software system to determine ENOB of ADC under test is presented in Fig. 1.

The system offered allows implementing both methods with the help of standard hardware based on personal computer (**PC**), NI PCIe-6321 embedded data acquisition board, NI BNC-2120 connector block and virtual instruments in LabVIEW graphical programming environment. At the same time test methods are automated to the maximum to achieve high accuracy of setting informative parameters of test signals, algorithmic transformations, computational operations and evaluation of dynamic characteristics.

The method offered assumes the presence of two signal sources, two reference DAC being used for this. The signals from DAC outputs, viz. a slowly changing signal in wide dynamic range (reference voltage: U_{ref}) and a fast changing signal with constant amplitude (test signal: U_{test}), are summed by the adder Σ. The sum of these signals enters comparators K1 and K2, the other outputs of which receive threshold voltage levels U_{t1}, U_{t2}. At the moment when output voltage is between comparison thresholds the signal form ADC output is fixed.

Timing diagrams of test and reference signal fragments are given in Fig. 2.

Two-comparator measuring method is suitable when both external synchronization output and internal sample rate output are present.

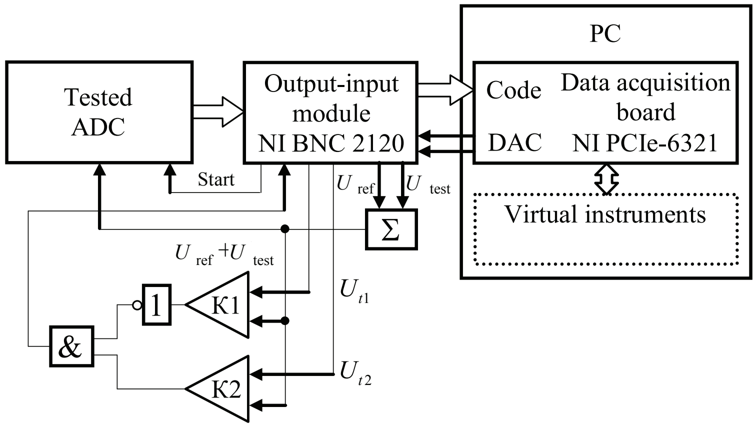

Fig. 1. The system for determining ENOB based on two comparators

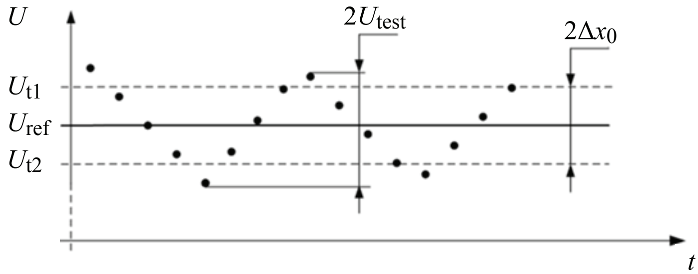

Fig. 2. Timing diagrams of the method to determine ENOB based on two comparators

Comparator thresholds are shifted relative to reference voltage by $\pm\Delta x_0$. Strobe-pulses for comparator state as well as trigger pulses of ADC converter (if external trigger is present) are applied periodically. The signal to permit registration of conversion results is formed only in the condition when the test signal superimposed on reference voltage is set in the interval of comparator thresholds.

If the analog-to-digital conversion has output of internal sampling rate the permission to register conversion results is formed by gating the comparators with internal trigger signals when converted signal is found between comparison thresholds. In two comparator method as well as test signal linear change within comparison results the average value coincides with reference signal $x_0 = U_{ref}$, the variance of which equals $\Delta x_0^2/3$ and is taken into consideration when processing measurement results.

The technique to measure ADC error in the mode of dynamic changes is as follows:

1) By means of reference DAC we set reference value $x_0 = Nq$, where N is code theoretical value that corresponds to input signal; q is quantization step;

2) Comparison thresholds spaced at $2x_0 = 2\Delta Nq$, where ΔN is code value that corresponds to threshold spaces relative to reference level are set;

3) The sum of reference voltage and test signal $(U_{ref} + U_{test})$ is formed;

4) The sum of reference voltage and test signal is supplied to the input of tested ADC and to the first inputs of comparator the second inputs of which are given comparison threshold voltages (U_{t1}, U_{t2});

5) Conversion result permitted by comparator states is registered when the signal converted is located in specified limits $x_0 \pm \Delta x_0$;

6) The errors of individual conversion results $\Delta i = (N_i - N)q$ are calculated;

7) Conversion results variance $D(\Delta) = \frac{1}{n}\sum_{i=1}^{n}(N_i - N)^2 q^2$, where n is the number of registered results is calculated;

8) Mean square value of error in the mode of dynamic changes is calculated $\sigma_\Delta = \sqrt{D(\Delta) - \Delta x_0^2/3}$;

9) $\text{ENOB} = N - \log_2 \frac{\sigma_\Delta}{\sigma_q}$, where σ_q is quantization error of ideal quantizer is calculated;

10) Test signal slew rate is changed, and the measurement process is repeated according to points 5) – 9);

11) New value of reference signal is set, the measurement process is repeated.

If converter input is given a signal with slew rate V_1, and converter one is given a signal with the rate V_2, then the error value measured has two components that have appeared due to the delays in converter and comparator:

$$\Delta_{1i} = \Delta_{n1i} - \Delta_{k1i},$$

where Δ_{1i} is error value in the first experiment (with the first combination of test signal slew rates); Δ_{n1i} is converter dynamic error value in the first experiment; Δ_{k1i} is comparator dynamic value in the first test.

Having performed four tests with different signal rates on the inputs of converter and comparator, having averaged the values received we get the system of equations to determine systematic errors of converter Δ_{ns} and comparator Δ_{ks}:

$$\overline{\Delta}_1 = \overline{\Delta}_{n1} + \overline{\Delta}_{k1};$$
$$\overline{\Delta}_2 = \overline{\Delta}_{n2} + \overline{\Delta}_{k1};$$
$$\overline{\Delta}_3 = \overline{\Delta}_{n1} + \overline{\Delta}_{k2};$$
$$\overline{\Delta}_4 = \overline{\Delta}_{n2} + \overline{\Delta}_{k2}.$$

The solution of the system of equations allows us to get the estimates of systematic error for the converter under consideration at two rates of input signal change V_1, V_2.

Having repeated the tests for other combinations of signal change rate we can build the dependency of dynamic error systematic component from the slew rate of input influence.

Conclusion

Methods of measuring ADC dynamic errors are offered and developed. Further research in this direction should provide the implementation of the methods elaborated into the verification practice of metrological organizations.

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Методы определения динамических характеристик интегральных АЦП

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Ключевые слова: дифференциальная нелинейность; динамические характеристики; эффективное число разрядов; мгновенные динамические погрешности; интегральные АЦП; интегральная нелинейность.

Аннотация: Предложены методы определения мгновенных динамических погрешностей интегральных аналого-цифровых преобразователей и эффективного числа разрядов. Первый метод заключается в сравнении зарегистрированного сигнала известной формы на выходе испытываемого АЦП, с моделью этой формы, формируемой с помощью ЭВМ. Эффективное число разрядов определяется по экспериментальным данным через погрешность, возникающую в каждой точке динамического диапазона АЦП, в зависимости от заданной скорости изменения испытательного сигнала или его частоты.

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Methoden zur Bestimmung der dynamischen Eigenschaften von Integral-ADCs

Zusammenfassung: Es sind Methoden zur Bestimmung der momentanen dynamischen Fehler von integralen Analog-Digital-Wandlern und der effektiven Anzahl von Entladungen vorgeschlagen. Die erste Methode besteht darin, das registrierte Signal einer bekannten Form am Ausgang des getesteten ADC mit einem von einem Computer erzeugten Modell dieser Form zu vergleichen. Die effektive Anzahl der Entladungen wird anhand der experimentellen Daten durch den Fehler bestimmt, der an jedem Punkt des Dynamikbereichs des ADC auftritt, abhängig von der festgelegten Änderungsrate des Testsignals oder seiner Frequenz.

Méthodes de la détermination des caractéristiques dynamiques des convertisseurs analogiques numériques

Résumé: Sont proposées des méthodes pour déterminer les erreurs dynamiques instantanées des convertisseurs analogiques numériques intégrés et le nombre effectif des bits. La première méthode consiste à comparer le signal enregistré d'une forme connue à la sortie du convertisseur analogique numérique testé avec un modèle de cette forme généré par ordinateur. Le nombre effectif des bits est déterminé à partir des données expérimentales par l'erreur qui se produit à chaque point de la plage dynamique du convertisseur analogique numériques intégré en fonction du taux de variation du signal d'essai ou de sa fréquence.

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